Solar Panel Manufacturing Process Explained Step-by-Step

A comprehensive breakdown of automated PV assembly.

Content Partner: J. v. G. technology GmbH

Turnkey solar module production lines — since 1997

www.jvg-thoma.com

A Technical Overview of the Solar Panel Manufacturing Process

Created as part of the PVKnowHow Knowledge Network

Prepared by J.v.G. Technology GmbH

European specialists in turnkey solar module production lines

Market Growth & Cost Decline

Global Market Trajectory

- Solar PV additions have grown at ~27% CAGR from 2014–2024
- Global module manufacturing capacity projected to reach 1.8 TW by end of 2025
- China accounts for the majority of supply chain capacity
- Market shifting from subsidy-driven to competitive pricing (PPAs)

Cost Decline Trend

- Global average module selling price: ~$0.13/Wp in 2024
- Average project capex dropped from ~$3,000/kW (2014–2016) to ~$1,000/kW (2024–2026)
- Silicon usage reduced from ~16 g/Wp (2004) to ~2 g/Wp (2024)
- PV forecast to achieve lowest LCOE globally by 2030

Source: Fraunhofer ISE Photovoltaics Report / Climate Energy Finance (CEF) / IRENA

Competitive Landscape: Global Players

China — Dominant Supply Chain

- Controls ingot, wafer, cell, and module production stages
- 29% manufacturing capacity growth in 2024 alone
- Aggressive scaling and close cooperation with equipment suppliers
- Overcapacity driving record-low module prices

Southeast Asia — Secondary Hub

- ~35–45 GW of wafer facilities in operation by end of 2024
- Key staging point for non-Chinese wafer production
- Proximity advantages for export markets

Europe & North America — Re-emerging

- Policy-driven reshoring initiatives underway
- US imposing tariffs on Chinese PV products
- EU driving localized, carbon-efficient supply chains
- High barriers for ingot/wafer re-establishment

Types of Solar Panels: Overview

Monocrystalline Silicon

- Single-crystal silicon structure
- Highest efficiency: ~20–25%+
- Dominant market technology
- Czochralski growth process

Polycrystalline Silicon

- Multi-grain silicon structure
- Efficiency: ~15–20%
- Lower manufacturing cost than mono
- Directional solidification process

Thin-Film

- CdTe, CIGS, amorphous silicon (a-Si)
- Efficiency: ~10–19% (technology-dependent)
- Lower material usage; flexible substrates
- ~10% global market share

Silicon wafer-based technology accounts for ~98% of total global PV production as of 2024. Source: Fraunhofer ISE / ITRPV

Monocrystalline Silicon: Key Characteristics

Technology Profile

- Produced via the Czochralski (Cz) process
- Single continuous crystal lattice — minimal grain boundaries
- Wafer size up to 210mm (M12 format)
- N-type wafers: ~70% market share in 2024
- Highest recorded efficiency: 26.7% (lab)

Manufacturing & Performance Factors

- Higher energy input required for crystal growth
- Diamond wire sawing to ~140 µm wafer thickness (2024)
- Temperature coefficient: ~−0.45%/°C
- Commercially dominant — outcompeted polycrystalline on cost-efficiency
- Preferred for space-constrained, high-performance applications

Polycrystalline Silicon: Key Characteristics

Technology Profile

- Produced via directional solidification (DSS process)
- Multi-grain crystal structure — visible blue hue
- Less energy-intensive to produce than monocrystalline
- Efficiency range: ~15–20% commercially
- Highest recorded efficiency: 24.4% (lab)

Market Status

- Declining market share — monocrystalline now dominant in c-Si
- Lower per-unit cost historically; advantage eroded by mono improvements
- Temperature coefficient: ~−0.39%/°C
- Still viable in cost-sensitive, large-area utility projects
- Wafers pre-doped with boron (p-type) as standard

Thin-Film: Key Characteristics

CdTe (Cadmium Telluride)

- Efficiency: ~17–19% commercial; 22.1% lab record
- Lowest cost per watt in thin-film category
- Dominant thin-film technology (~5% global PV market)
- Strong temperature performance; low coefficient vs. c-Si
- Cadmium toxicity requires careful handling and end-of-life recycling

CIGS (Copper Indium Gallium Selenide)

- Efficiency: ~12–16% commercial; 23.64% lab record
- Flexible substrates — suitable for BIPV and portable applications
- Better low-light and high-temperature performance vs. c-Si
- Complex four-element composition; higher manufacturing difficulty
- ~2% global PV market share

Amorphous Silicon (a-Si)

- Efficiency: ~8–10% commercially
- Most flexible and lightweight; deposited on glass, plastic, or metal
- Consistent output under partial shading and diffuse light
- Subject to light-induced degradation (Staebler-Wronski effect)
- Suited for low-power, specialty, and BIPV applications

Silicon vs. Thin-Film: Comparative Analysis

Parameter	Monocrystalline Si	Polycrystalline Si	Thin-Film (CdTe/CIGS)
Commercial Efficiency	20–25%+	15–20%	10–19% (varies by type)
Market Share (2024)	~70% (n-type dominant)	Declining	~10% total thin-film
Manufacturing Cost	Higher (Cz process)	Moderate	Low–moderate
Temperature Performance	Moderate (−0.45%/°C)	Moderate (−0.39%/°C)	Better (CdTe −0.32%/°C)
Flexibility / Form Factor	Rigid wafer	Rigid wafer	Flexible substrates possible
Typical Application	Residential, utility-scale	Utility, cost-driven projects	Utility (CdTe), BIPV (CIGS)

Silicon wafer-based technology (~98% of global production) dominates due to cost-efficiency improvements. Source: Fraunhofer ISE / Wikipedia

Efficiency Drivers in PV Manufacturing

Wafer Quality

- Purity of silicon feedstock (solar-grade vs. electronic-grade)
- Crystal perfection — fewer grain boundaries = higher efficiency
- Wafer thickness: thinner wafers (140 µm) reduce material cost
- Larger wafer formats (M10, M12) increase cell power output

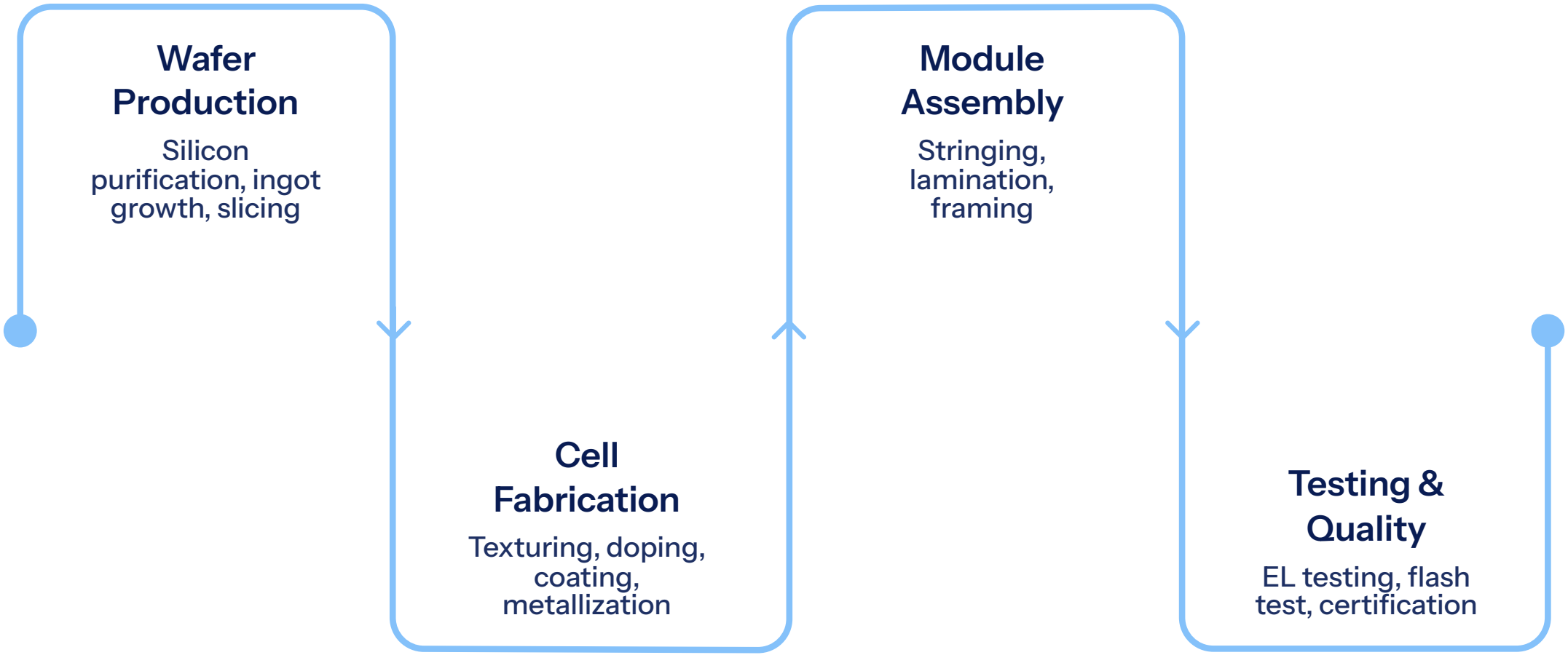
Cell Processing Precision

- Surface texturing reduces optical reflection losses
- Diffusion doping controls p-n junction quality
- Anti-reflective coating (silicon nitride via PECVD)
- Metallization contact printing accuracy (silver paste)

Module Assembly & Materials

- Encapsulant (EVA) quality affects UV and thermal stability
- Tabbing and stringing precision minimizes resistive losses
- Lamination process parameters control adhesion and durability
- Junction box quality impacts electrical reliability

Manufacturing Process Overview



The full manufacturing chain from raw silicon to market-ready module spans four integrated process stages, each governed by strict process parameters and quality checkpoints. Materials dominate the cost structure (~95% of total production cost), making procurement and process yield the primary operational levers.

Wafer Production

1

Silicon Purification

Quartz → metallurgical-grade Si → Siemens process → high-purity polysilicon feedstock

2

Ingot Growth

Czochralski (mono) or directional solidification (poly); seed crystal guides crystal formation under controlled temperature

3

Wafer Slicing

Diamond wire saws cut ingots to ~140 µm wafers; kerf (silicon dust) is a recoverable by-product

4

Wafer Prep

Lapping, etching, and cleaning remove surface damage; wafers sorted by quality before cell fabrication

Ingot and wafer production is the most capital-intensive and geographically concentrated stage — predominantly in China and Southeast Asia.

Cell Production

01

Surface Texturing

KOH chemical etching creates pyramid-like surface microstructure — reduces optical reflection and traps more incident light

02

Diffusion Doping

Phosphorus or boron doping in diffusion furnace creates the p-n junction — the electrical engine of the photovoltaic effect

03

Anti-Reflective Coating

Silicon nitride applied via PECVD — reduces surface reflection, passivates surface defects, and improves carrier lifetime

04

Metallization & Testing

Screen-printed silver contacts collect current; each cell tested for efficiency and electrical output before assembly

Module Assembly

1

Tabbing & Stringing

Copper ribbons solder cells in series; automated stringing machines align and connect cells to form strings at target voltage

2

Lay-Up & Encapsulation

Cell strings arranged on tempered glass; EVA encapsulant sheets placed above and below for moisture and mechanical protection

3

Lamination

Heat and vacuum press bonds all layers; critical process parameter — temperature, pressure, and time define long-term adhesion quality

4

Framing & Junction Box

Aluminum frame provides structural rigidity; junction box with bypass diodes fitted to rear; modules ready for testing

Key materials: tempered glass, EVA encapsulant, backsheet, aluminum frame, junction box — components that together account for the bulk of material cost.

Testing & Quality Control

Flash / STC Testing

- Simulated solar irradiance at Standard Test Conditions (STC: 1000 W/m^2, 25°C)
- Measures: power output, Voc, Isc, fill factor, efficiency
- Each module binned by power class

Electroluminescence (EL) Testing

- Camera imaging detects microcracks, broken cells, and internal defects
- Non-destructive — performed on 100% of production output
- Critical for detecting latent field failures

Mechanical & Environmental Tests

- Mechanical load: wind, snow, hail resistance simulation
- Thermal cycling and humidity-freeze tests
- Insulation resistance and dielectric withstand testing

Certifications & Standards

Core International Standards

- **IEC 61215** — Design qualification & performance; tests aging behavior under UV, temperature cycles, mechanical load, and humidity
- **IEC 61730** — Safety standard; covers electrical shock, fire hazard, and mechanical integrity — mandatory for virtually all commercial markets
- **IEC 61646** — Thin-film module qualification (now merged with IEC 61215)
- **IEC 61853** — Energy performance rating under varying irradiance and temperature conditions

Market Access & Bankability

- IEC 61215 + IEC 61730 certification is the baseline requirement for EU, Australian, and most Asian markets
- UL 61730 required for North American market access
- Without certification, modules excluded from utility-scale and financed projects
- TÜV Rheinland and similar bodies provide extended stress testing beyond IEC minimum
- Certification is type-approval — ongoing in-process quality control remains the manufacturer's responsibility

Source: IEC / J.v.G. Technology GmbH / TÜV Rheinland. Certification process typically takes several months including sample preparation, shipping, and laboratory testing.

Conclusion: Process & Quality as Competitive Advantage

Process Mastery Determines Output Quality

Each stage — wafer, cell, module — introduces variables that compound. Controlling texturing, doping, lamination, and metallization parameters directly determines efficiency, yield, and long-term reliability.

Materials Dominate Cost; Certification Unlocks Markets

At ~95% of total production cost, material procurement strategy is the central operational priority. IEC 61215 + IEC 61730 certification is the non-negotiable entry point to global commercial and financed markets.

Turnkey Methodologies Reduce Ramp Risk

Access to an established production methodology with documented process parameters — as offered by experienced European turnkey providers — significantly reduces technology risk and accelerates the path to certified, bankable production.

This presentation is based on publicly available technical data and composite scenario analysis. Source: PVKnowHow / J.v.G. Technology GmbH / Fraunhofer ISE / IEC

About the Content Partner

J. v. G. technology GmbH — The DESERT Company

Founded in 1997 in Bavaria, Germany. Family-owned engineering company specializing in turnkey solar module production lines.

More than 90 factory projects delivered worldwide.
On-site team training included — no prior manufacturing experience required.

Key areas:

Turnkey PV manufacturing lines | DESERT Technology® | TÜV-certified module designs | Factory planning to production

www.jvg-thoma.com

Contact

J.v.G. Technology GmbH

Möningerberg 1a, 92342 Freystadt, Germany

info@jvg-thoma.de | **www.jvg-thoma.com**

Source: https://www.pvknowhow.com/solar-panel-manufacturing-process/

Created with the support of JvGLabs — specialist for AI systems and AI-driven visibility. www.jvglabs.com